LM2653 1.5A High Efficiency Synchronous Switching Regulator

Check for Samples: LM2653

FEATURES

- **Efficiency up to 97%**
- **4V to 14V Input Voltage Range**
- **1.5V to 5.0V Adjustable Output Voltage**
- **0.1Ω Switch On Resistance**
- **300 kHz Fixed Frequency Internal Oscillator**
- **7 µA Shutdown Current**
- **Patented Current Sensing for Current Mode Control**
- **Input Undervoltage Lockout**
- **Output Overvoltage Shutdown Protection**
- **Output Undervoltage Shutdown Protection**
- **Adjustable Soft-Start**
- **Adjustable PGOOD Delay**
- **Current Limit and Thermal Shutdown**

APPLICATIONS

- **Webpad**
- **Personal Digital Assistants (PDAs)**
- **Computer Peripherals**
- **Battery-Powered Devices**
- **Notebook Computer Video Supply**
- **Handheld Scanners**
- **GXM I/O and Core Voltage**
- **High Efficiency 5V Conversion**

DESCRIPTION

The LM2653 switching regulator provides high efficient power conversion over a 100:1 load range (1.5A to 15 mA). This feature makes the LM2653 an ideal fit in battery-powered applications.

Synchronous rectification is used to achieve up to 97% efficiency. At light loads, the LM2653 enters a low power hysteretic or “sleep” mode to keep the efficiency high. In many applications, the efficiency still exceeds 80% at 15 mA load. A shutdown pin is available to disable the LM2653 and reduce the supply current to 7µA.

All the power, control, and drive functions are integrated within the ICs. The ICs contain patented current sensing circuity for current mode control. This feature eliminates the external current sensing resistor required by other current-mode DC-DC converters.

The ICs have a 300 kHz fixed frequency internal oscillator. The high oscillator frequency allows the use of extremely small, low profile components.

Protection features include thermal shutdown, input undervoltage lockout, adjustable soft-start, cycle by cycle current limit, output overvoltage and undervoltage protections.

Typical Application

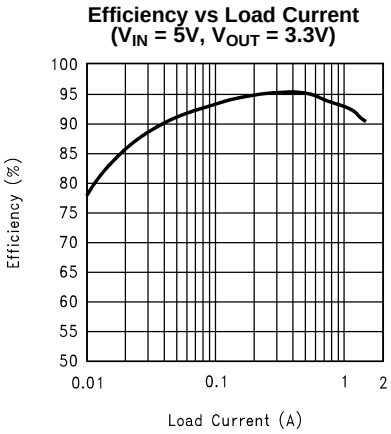

Figure 1.

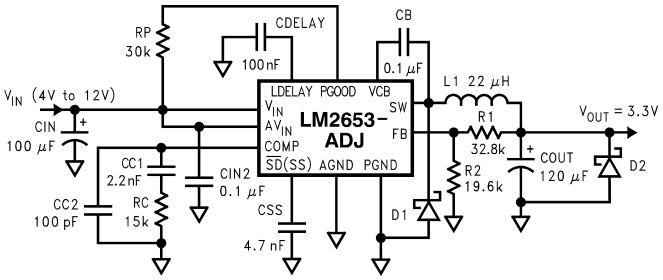

Figure 2.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2][3]

Input Voltage			15V
PGOOD Pin Voltage			15V
Feedback Pin Voltage			−0.4V ≤ V_{FB} ≤ 5V
Power Dissipation (T_A =25°C) [4]			893 mW
Junction Temperature Range			−40°C ≤ T_J ≤ +125°C
Storage Temperature Range			−65°C to +150°C
Lead Temperature	PW Package	Vapor Phase (60 sec.)	215°C
		Infrared (15 sec.)	220°C
Maximum Junction Temperature			150°C
ESD Susceptibility		Human Body Model [3]	1 kV

(1) Absolute Maxmum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but device parameter specifications may not be specified under these conditions. For specified specifications and test conditions, see Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin.
(4) The maximum allowable power dissipation is calculated by using $P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA}$, where T_{JMAX} is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance of the specified package. The 893 mW rating results from using 150°C, 25°C, and 140°C/W for T_{JMAX}, T_A, and θ_{JA} respectively. A θ_{JA} of 140°C/W represents the worst-case condition of no heat sinking of the 16-pin TSSOP package. Heat sinking allows the safe dissipation of more power. The Absolute Maximum power dissipation must be derated by 7.14 mW per °C above 25°C ambient. The LM2653 actively limits its junction temperatures to about 165°C.

Operating Ratings[1]

Supply Voltage	4V ≤ V_{IN} ≤ 14V

(1) Absolute Maxmum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but device parameter specifications may not be specified under these conditions. For specified specifications and test conditions, see Electrical Characteristics.

Electrical Characteristics

Specifications with standard typeface are for T_J = 25°C, and those in **boldface type** apply over full **Operating Temperature Range**. V_{IN} = 10V unless otherwise specified.

Symbol	Parameter	Conditions	Typical [1]	Limit [2]	Units
V_{FB}	Feedback Voltage	I_{LOAD} = 900 mA	1.238	**1.200** **1.263**	V V(min) V(max)
V_{OUT}	Output Voltage Line Regulation	V_{IN} = 4V to 12V I_{LOAD} = 900 mA	0.2		%
	Output Voltage Load Regulation	I_{LOAD} = 10 mA to 1.5A V_{IN} = 5V	1.3		%
	Output Voltage Load Regulation	I_{LOAD} = 200 mA to 1.5A V_{IN} = 5V	0.3		%
V_{INUV}	V_{IN} Undervoltage Lockout Threshold Voltage	Rising Edge	3.8	**3.95**	V V(max)
V_{UV_HYST}	Hysteresis for the Input Undervoltage Lockout		210		mV
I_{CL}	Switch Current Limit	V_{IN} = 5V V_{OUT} = 2.5V	2.0	**1.55** **2.60**	A A(min) A(max)
I_{SM}	Sleep Mode Threshold Current	V_{IN} = 5V, V_{OUT} = 2.5V	100		mA

(1) All limits specified at room temperature (standard typeface) and at **temperature extremes (bold typeface)**. All room temperature limits are 100% production tested. All limits at **temperature extremes** are specified via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) Typical numbers are at 25°C and represent the most likely norm.

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Electrical Characteristics (continued)

Specifications with standard typeface are for T_J = 25°C, and those in **boldface type** apply over full **Operating Temperature Range**. V_{IN} = 10V unless otherwise specified.

Symbol	Parameter	Conditions	Typical (1)	Limit (2)	Units
V_{HYST}	Sleep Mode Feedback Voltage Hysteresis		24		mV
I_Q	Quiescent Current		1.7	**2.0**	mA mA(max)
I_{QSD}	Quiescent Current in Shutdown Mode	Shutdown Pin Pulled Low	7	12/**20**	µA µA(max)
$R_{DS(ON)}$	High-Side or Low-Side MOSFET ON Resistance	I_{SWITCH} = 1A	75	**130**	mΩ mΩ (max)
$R_{SW(ON)}$	High-Side or Low-Side Switch On Resistance (MOSFET ON Resistance + Bonding Wire Resitstance)	I_{SWITCH} = 1A	110		mΩ
I_L	Switch Leakage Current—High Side		130		nA
	Switch Leakge Current—Low Side		130		nA
V_{BOOT}	Bootstrap Regulator Voltage	I_{BOOT} = 1 mA	6.75	6.45/**6.40** 6.95/**7.00**	V V(min) V(max)
G_M	Error Amplifier Transconductance		1250		µmho
A_V	Error Amplifier Voltage Gain		100		
I_{EA_SOURCE}	Error Amplifier Source Current	V_{IN} = 3.6V, V_{FB} = 1.17V, V_{COMP} = 2V	40	25/**15**	µA µA(min)
I_{EA_SINK}	Error Amplifier Sink Current	V_{IN} = 3.6V, V_{FB} = 1.31V, V_{COMP} = 2V	65	**30**	µA µA(min)
V_{EAH}	Error Amplifier Output Swing Upper Limit	V_{IN} = 4V, V_{FB} = 1.17V	2.70	2.50/**2.40**	V V(min)
V_{EAL}	Error Amplifier Output Swing Lower Limit	V_{IN} = 4V, V_{FB} = 1.31V	1.25	1.35/**1.50**	V V(max)
V_D	Body Diode Voltage	I_{DIODE} = 1.5A	1		V
F_{OSC}	Oscillator Frequency	Measured at Switch Pin V_{IN} = 4V	300	280/**255** 330/**345**	kHz kHz(min) kHz(max)
D_{MAX}	Maximum Duty Cycle	V_{IN} = 4V	95	**92**	% %(min)
I_{SS}	Soft-Start Current	Voltage at the SS Pin = 1.4V	11	**7** **14**	µA µA(min) µA(max)
V_{OUTUV}	V_{OUT} Undervoltage Lockout Threshold Voltage		81	**76** **84**	$\%V_{OUT}$ $\%V_{OUT}$(min) $\%V_{OUT}$(max)
	Hysteresis for V_{OUTUV}		5		$\%V_{OUT}$
V_{OUTOV}	V_{OUT} Overvoltage Lockout Threshold Voltage		108	**106** **114**	$\%V_{OUT}$ $\%V_{OUT}$(min) $\%V_{OUT}$(max)
	Hysteresis for V_{OUTOV}		3		$\%V_{OUT}$
$I_{LDELAY—SOURCE}$	LDELAY Pin Source Current		5		µA
$I_{PGOOD—SINK}$	PGOOD Pin Sink Current	V_{PGOOD} = 0.4V		**15**	mA(max)
$I_{PGOOD—LEAKAGE}$	PGOOD Pin Leakage Current	V_{PGOOD} = 5V	50		nA
$I_{SHUTDOWN}$	Shutdown Pin Current	Shutdown Pin Pulled Low	2.2	0.8/**0.5** 3.7/**4.0**	µA µA(min) µA(max)

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Electrical Characteristics (continued)

Specifications with standard typeface are for T_J = 25°C, and those in **boldface type** apply over full **Operating Temperature Range**. V_{IN} = 10V unless otherwise specified.

Symbol	Parameter	Conditions	Typical (1)	Limit (2)	Units
$V_{SHUTDOWN}$	Shutdown Pin Threshold Voltage	Rising Edge	0.6	**0.3** **0.9**	V V(min) V(max)
T_{SD}	Thermal Shutdown Temperature		165		°C
T_{SD_HYST}	Thermal Shutdown Hysteresis Temperature		25		°C

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Typical Performance Characteristics

Efficiency vs Load Current (V_{IN} = 5V, V_{OUT} = 2.5V)

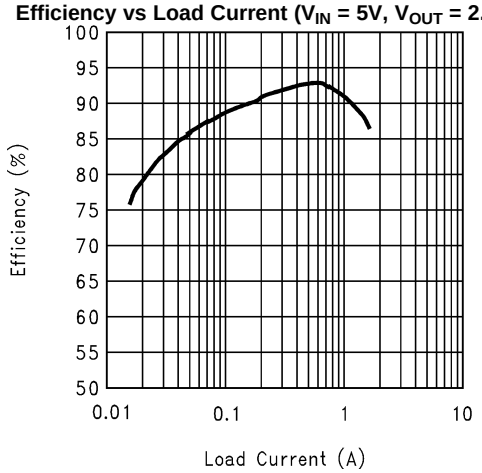

Figure 3.

I_Q vs V_{IN}

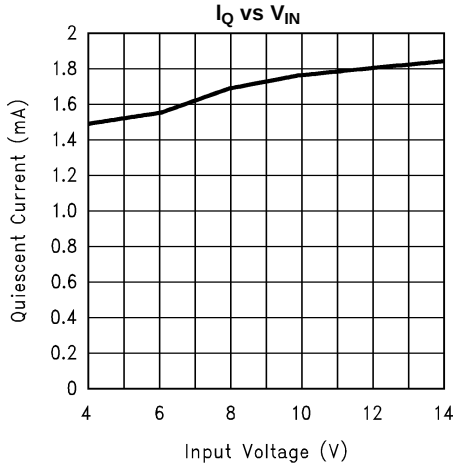

Figure 4.

I_{QSD} vs Input Voltage

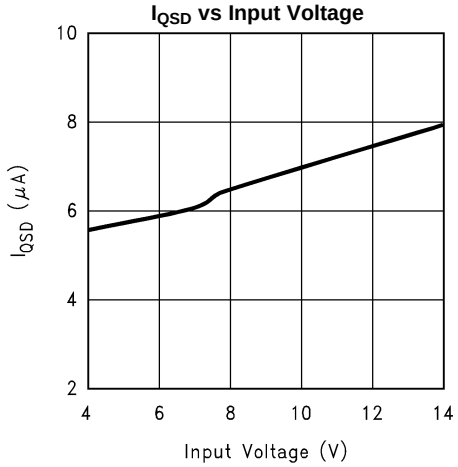

Figure 5.

I_{QSD} vs Junction Temperature

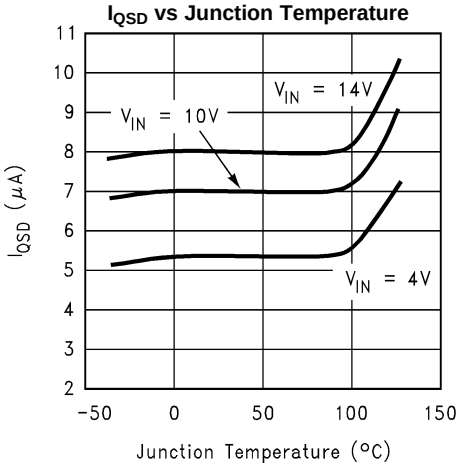

Figure 6.

Frequency vs Junction Temperature

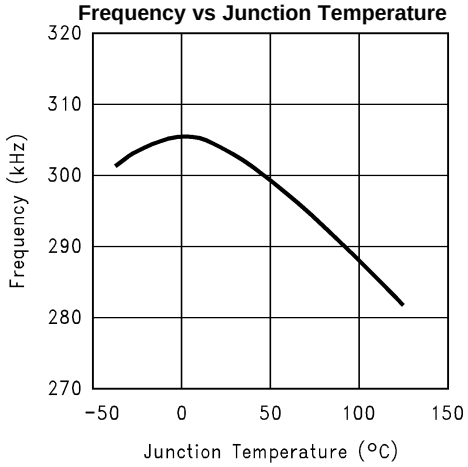

Figure 7.

$R_{SW(ON)}$ vs Input Voltage

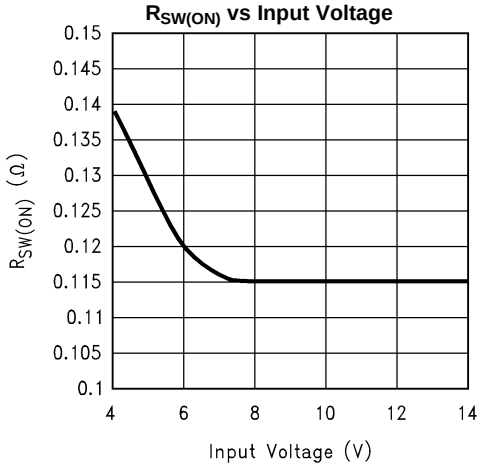

Figure 8.

Typical Performance Characteristics (continued)

$R_{SW(ON)}$ vs Junction Temperature

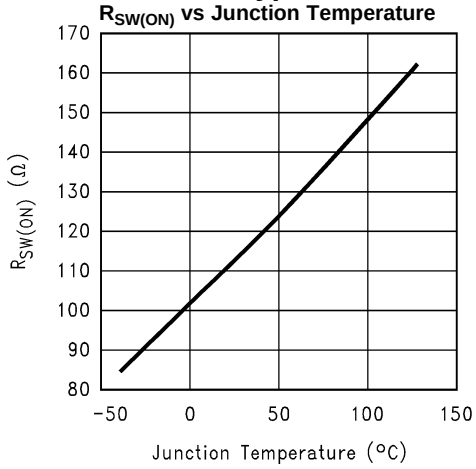

Figure 9.

Current Limit vs Input Voltage (V_{OUT} = 2.5V)

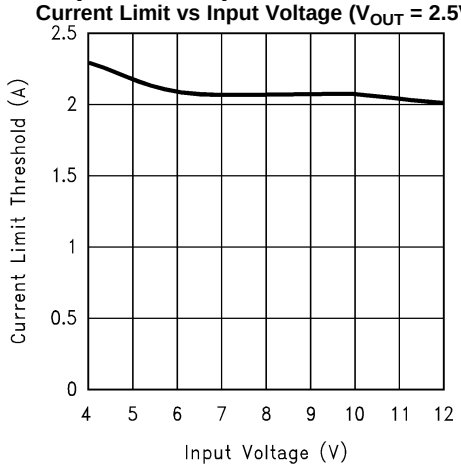

Figure 10.

Current Limit vs Junction Temperature (V_{OUT} = 2.5V)

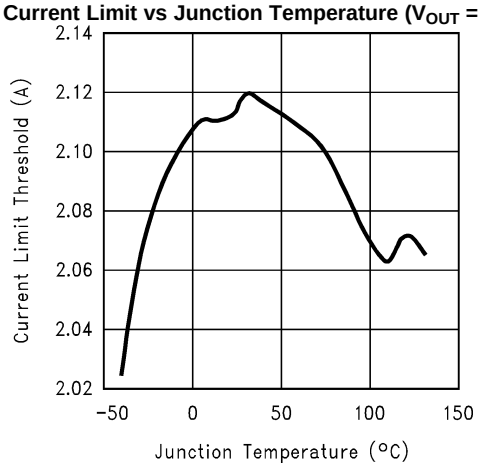

Figure 11.

Reference Voltage vs Junction Temperature

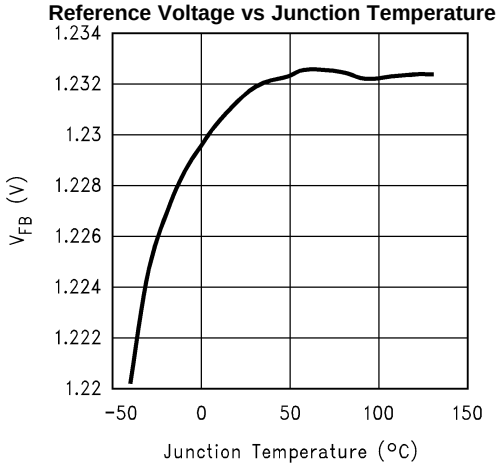

Figure 12.

Sleep Mode Threshold vs Output Voltage (V_{IN} = 5V)

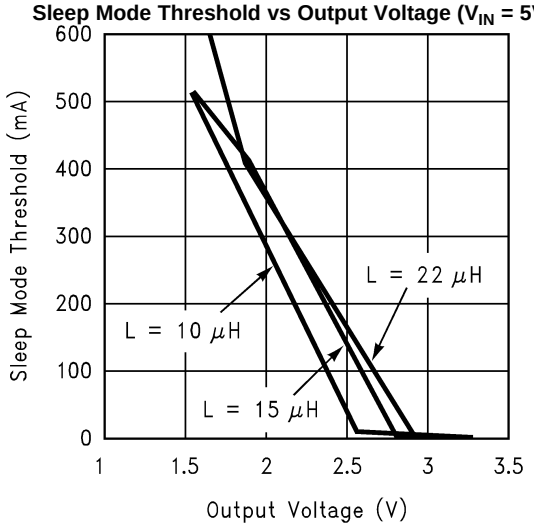

Figure 13.

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CONNECTION DIAGRAM

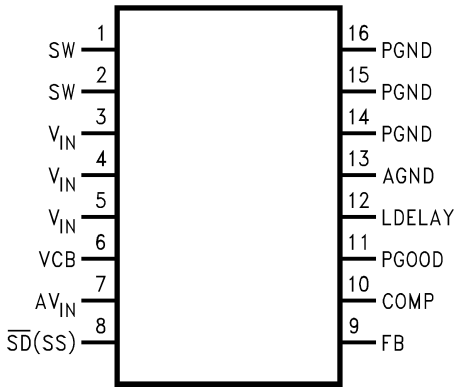

Figure 14. 16-Lead TSSOP (PW)
See Package Number PW0016A

PIN DESCRIPTIONS

Pin	Name	Function
1-2	SW	Switched-node connection, which is connected with the source of the internal high-side MOSFET.
3-5	V_{IN}	Main power supply input pin. Connected to the drain of the high-side MOSFET.
6	V_{CB}	Bootstrap capacitor connection for high-side gate drive.
7	AV_{IN}	Input voltage for control and driver circuits.
8	$\overline{SD}$(SS)	Shutdown and Soft-start control pin. Pulling this pin below 0.3V shuts off the regulator. A capacitor connected from this pin to ground provides a control ramp of the input current. Do not drive this pin with an external source or erroneous operation may result.
9	FB	Output voltage feedback input. Connected to the output voltage.
10	COMP	Compensation network connection. Connected to the output of the voltage error amplifier.
11	PGOOD	A constant monitor on the output voltage. PGOOD will go low if the output voltage exceeds 110% or goes below 80% of its nominal.
12	LDELAY	A capacitor between this pin to ground sets the delay from the output voltage reaches 80% of its nominal to when the undervoltage latch protection is enabled and PGOOD pin goes low.
13	AGND	Low-noise analog ground.
14-16	PGND	Power ground.

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Block Diagram

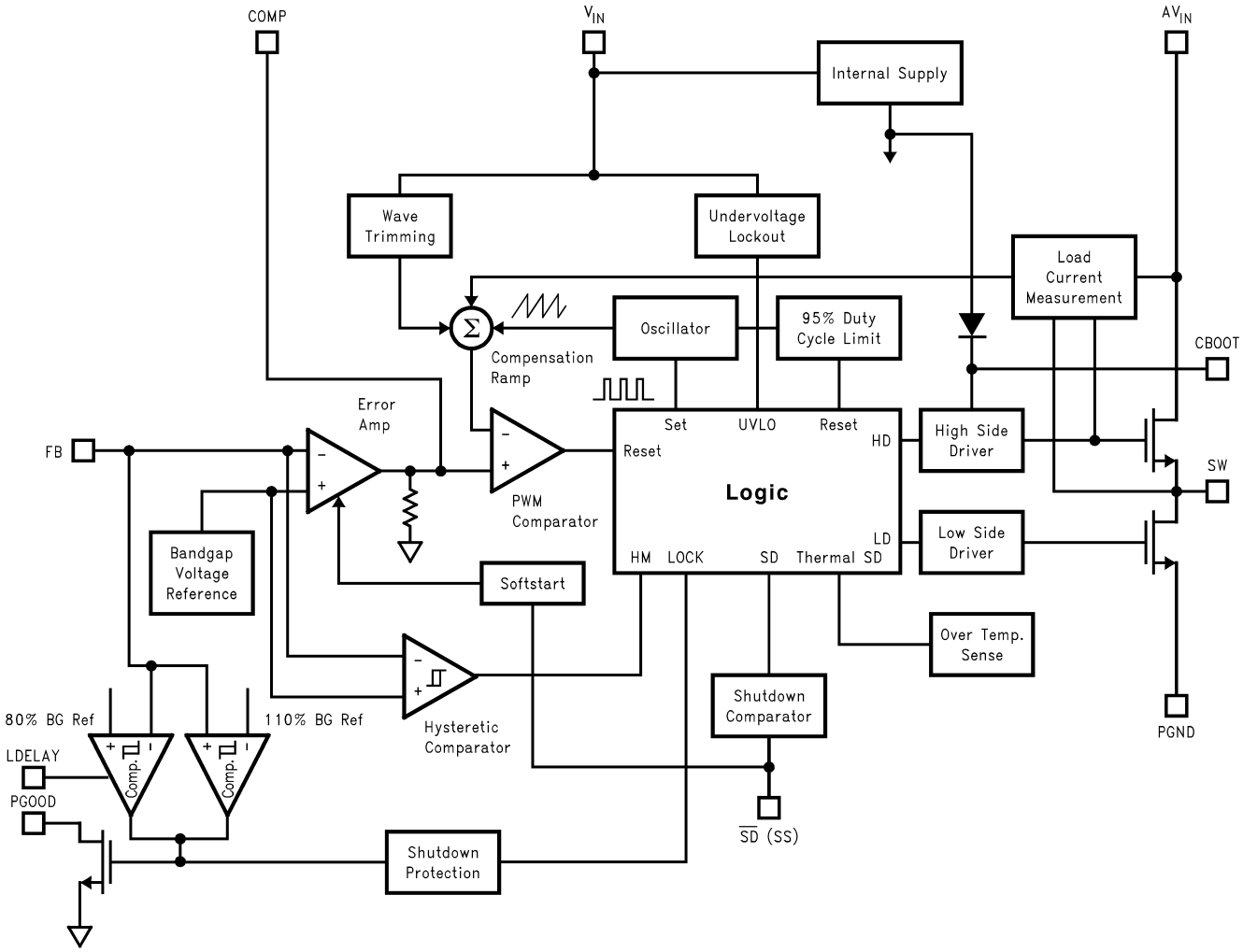

Figure 15.

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OPERATION

The LM2653 operates in a constant frequency (300 kHz), current-mode PWM for moderate to heavy loads; and it automatically switches to hysteretic mode for light loads. In hysteretic mode, the switching frequency is reduced to keep the efficiency high.

MAIN OPERATION

When the load current is higher than the sleep mode threshold, the part is always operating in PWM mode. At the beginning of each switching cycle, the high-side switch is turned on, the current from the high-side switch is sensed and compared with the output of the error amplifier (COMP pin). When the sensed current reaches the COMP pin voltage level, the high-side switch is turned off; after 40 ns (deadtime), the low-side switch is turned on. At the end of the switching cycle, the low-side switch is turned off; and the same cycle repeats.

The current of the top switch is sensed by a patented internal circuitry. This unique technique gets rid of the external sense resistor, saves cost and size, and improves noise immunity of the sensed current. A feedforward from the input voltage is added to reduce the variation of the current limit over the input voltage range.

When the load current decreases below the sleep mode theshold, the output voltage will rise slightly, this rise is sensed by the hysteretic mode comparator which makes the part go into the hysteretic mode with both the high and low side switches off. The output voltage starts to drop until it hits the low threshold of the hysteretic comparator, and the part immediately goes back to the PWM operation. The output voltage keeps increasing until it reaches the top hysteretic threshold, then both the high and low side switches turn off again, and th same cycle repeats.

PROTECTIONS

The cycle-by-cycle current limit circuitry turns off the high-side MOSFET whenever the current in MOSFET reaches 2A. A second level current limit is accomplished by the undervoltage protection: if the load pulls the output voltage down below 80% of its nominal value, the undervoltage latch protection will wait for a period of time (set by the capacitor at the LDELAY pin, see LDELAY CAPACITOR for more information). If the output voltage is still below 80% of its nominal after the waiting period, the latch protection will be enabled. In the latch protection mode, the low-side MOSFET is on and the high-side MOSFET is off. The latch protection will also be enabled immediately whenever the output voltage exceeds the overvoltage threshold (110% of its nominal). Both protections are disabled during start-up.(See SOFT-START CAPACITOR and LDELAY CAPACITOR for more information.) Toggling the input supply voltage or the shutdown pin can reset the device from the latched protection mode.

PGOOD FLAG

The PGOOD flag goes low whenever the overvoltage or undervoltage latch protection is enabled.

Design Procedure

This section presents guidelines for selecting external components.

INPUT CAPACITOR

A low ESR aluminum, tantalum, or ceramic capacitor is needed between the input pin and power ground. This capacitor prevents large voltage transients from appearing at the input. The capacitor is selected based on the RMS current and voltage requirements. The RMS current is given by:

$$I_{RMS} = I_{OUT} \times \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}} \tag{1}$$

The RMS current reaches its maximum ($I_{OUT}/2$) when V_{IN} equals $2V_{OUT}$. For an aluminum or ceramic capacitor, the voltage rating should be at least 25% higher than the maximum input voltage. If a tantalum capacitor is used, the voltage rating required is about twice the maximum input voltage. The tantalum capacitor should be surge current tested by the manufacturer to prevent shorted by the inrush current. It is also recommended to put a small ceramic capacitor (0.1 µF) between the input pin and ground pin to reduce high frequency spikes.

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INDUCTOR

The most critical parameters for the inductor are the inductance, peak current and the DC resistance. The inductance is related to the peak-to-peak inductor ripple current, the input and the output voltages:

$$L = \frac{(V_{IN} - V_{OUT})V_{OUT}}{V_{IN} \times I_{RIPPLE} \times 300\ kHz} \quad (2)$$

A higher value of ripple current reduces inductance, but increases the conductance loss, core loss, current stress for the inductor and switch devices. It also requires a bigger output capacitor for the same output voltage ripple requirement. A reasonable value is setting the ripple current to be 30% of the DC output current. Since the ripple current increases with the input voltage, the maximum input voltage is always used to determine the inductance. The DC resistance of the inductor is a key parameter for the efficiency. Lower DC resistance is available with a bigger winding area. A good tradeoff between the efficiency and the core size is letting the inductor copper loss equal 2% of the output power.

OUTPUT CAPACITOR

The selection of C_{OUT} is driven by the maximum allowable output voltage ripple. The output ripple in the constant frequency, PWM mode is approximated by:

$$V_{RIPPLE} = I_{RIPPLE}\left(ESR + \frac{1}{8F_S C_{OUT}}\right) \quad (3)$$

The ESR term usually plays the dominant role in determining the voltage ripple. A low ESR aluminum electrolytic or tantalum capacitor (such as Nichicon PL series, Sanyo OS-CON, Sprague 593D, 594D, AVX TPS, and CDE polymer aluminum) is recommended. An electrolytic capacitor is not recommended for temperatures below −25°C since its ESR rises dramatically at cold temperature. A tantalum capacitor has a much better ESR specification at cold temperature and is preferred for low temperature applications.

The output voltage ripple in constant frequency mode has to be less than the sleep mode voltage hysteresis to avoid entering the sleep mode at full load:

$$V_{RIPPLE} < 20mV * V_{OUT} / V_{FB} \quad (4)$$

BOOST CAPACITOR

A 0.1 µF ceramic capacitor is recommended for the boost capacitor. The typical voltage across the boost capacitor is 6.7V.

SOFT-START CAPACITOR

A soft-start capacitor is used to provide the soft-start feature. When the input voltage is first applied, or when the $\overline{SD}$(SS) pin is allowed to go high, the soft-start capacitor is charged by a current source (approximately 2 µA). When the $\overline{SD}$(SS) pin voltage reaches 0.6V (shutdown threshold), the internal regulator circuitry starts to operate. The current charging the soft-start capacitor increases from 2 µA to approximately 10 µA. With the $\overline{SD}$(SS) pin voltage between 0.6V and 1.3V, the level of the current limit is zero, which means the output voltage is still zero. When the $\overline{SD}$(SS) pin voltage increases beyond 1.3V, the current limit starts to increase. The switch duty cycle, which is controlled by the level of the current limit, starts with narrow pulses and gradually gets wider. At the same time, the output voltage of the converter increases towards the nominal value, which brings down the output voltage of the error amplifier. When the output of the error amplifier is less than the current limit voltage, it takes over the control of the duty cycle. The converter enters the normal current-mode PWM operation. The $\overline{SD}$(SS) pin voltage is eventually charged up to about 2V.

The soft-start time can be estimated as:

$$T_{SS} = C_{SS} * 0.6V/2\ \mu A + C_{SS} * (2V-0.6V)/10\ \mu A \quad (5)$$

During start-up, the internal circuit is monitoring the soft-start voltage. When the softstart voltage reaches 2V, the undervoltage and overvoltage protections are enabled.

If the output voltage doesn't rise above 80% of the normal value before the soft-start reaches 2V. The undervoltage protection will kick in and shut the device down. You can avoid this by either increasing the value of the soft-start capacitor, or using a LDELAY capacitor.

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LDELAY CAPACITOR

As mentioned in the Operation section, the LDELAY capacitor sets the time delay between the output voltage goes below 80% of its nominal value and the undervoltage latch protection is enabled.

Charging the CDELAY by a 5 µA current source up to 2V sets the delay time. Therefore, $T_{DELAY} = C_{DELAY}$ * 2V/5µA.

The undervoltage protection is disabled by tying the LDELAY pin to the ground.

R_1 and R_2 (PROGRAMMING OUTPUT VOLTAGE)

Use the following formula to select the appropriate resistor values:

$V_{OUT} = V_{REF}(1 + R_1/R_2)$

where

- $V_{REF} = 1.238V$ (6)

Select resistors between 10kΩ and 100kΩ. (1% or higher accuracy metal film resistors for R_1 and R_2.)

COMPENSATION COMPONENTS

In the control to output transfer function, the first pole F_{p1} can be estimated as $1/(2\pi R_{OUT}C_{OUT})$; The ESR zero F_{z1} of the output capacitor is $1/(2\pi ESRC_{OUT})$; Also, there is a high frequency pole F_{p2} in the range of 45kHz to 150kHz:

$F_{p2} = F_s/(\pi n(1-D))$

where

- $D = V_{OUT}/V_{IN}$
- $n = 1+0.348L/(V_{IN}-V_{OUT})$ (L is in µHs and V_{IN} and V_{OUT} in volts) (7)

The total loop gain G is approximately $500/I_{OUT}$ where I_{OUT} is in amperes.

A Gm amplifier is used inside the LM2653. The output resistor R_o of the Gm amplifier is about 80kΩ. C_{c1} and R_C together with R_o give a lag compensation to roll off the gain:

$F_{pc1} = 1/(2\pi C_{c1}(R_o+R_c))$, $F_{zc1} = 1/2\pi C_{c1}R_c$. (8)

In some applications, the ESR zero F_{z1} cannot be cancelled by F_{p2}. Then, C_{c2} is needed to introduce F_{pc2} to cancel the ESR zero, $F_{p2} = 1/(2\pi C_{c2}R_o \| R_c)$.

The rule of thumb is to have more than 45° phase margin at the crossover frequency (G=1).

If C_{OUT} is higher than 68µF, C_{c1} = 2.2nF, and R_c = 15KΩ are good choices for most applications. If the ESR zero is too low to be cancelled by F_{p2}, add C_{c2}.

If the transient response to a step load is important, choose R_C to be higher than 10kΩ.

EXTERNAL SCHOTTKY DIODE

A Schottky diode D_1 is recommended to prevent the intrinsic body diode of the low-side MOSFET from conducting during the deadtime in PWM operation and hysteretic mode when both MOSFETs are off. If the body diode turns on, there is extra power dissipation in the body diode because of the reverse-recovery current and higher forward voltage; the high-side MOSFET also has more switching loss since the negative diode reverse-recovery current appears as the high-side MOSFET turn-on current in addition to the load current. These losses degrade the efficiency by 1-2%. The improved efficiency and noise immunity with the Schottky diode become more obvious with increasing input voltage and load current.

The breakdown voltage rating of D_1 is preferred to be 25% higher than the maximum input voltage. Since D_1 is only on for a short period of time, the average current rating for D_1 only requires being higher than 30% of the maximum output current. It is important to place D_1 very close to the drain and source of the low-side MOSFET, extra parasitic inductance in the parallel loop will slow the turn-on of D_1 and direct the current through the body diode of the low-side MOSFET.

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PCB Layout Considerations

Layout is critical to reduce noises and ensure specified performance. The important guidelines are listed as follows:

1. Minimize the parasitic inductance in the loop of input capacitors and the internal MOSFETs by connecting the input capacitors to V_{IN} and PGND pins with short and wide traces. This is important because the rapidly switching current, together with wiring inductance can generate large voltage spikes that may result in noise problems.
2. Minimize the trace from the center of the output resistor divider to the FB pin and keep it away from noise sources to avoid noise pick up. For applications require tight regulation at the output, a dedicated sense trace (separated from the power trace) is recommended to connect the top of the resistor divider to the output.
3. If the Schottky diode D_1 is used, minimize the traces connecting D_1 to SW and PGND pins.

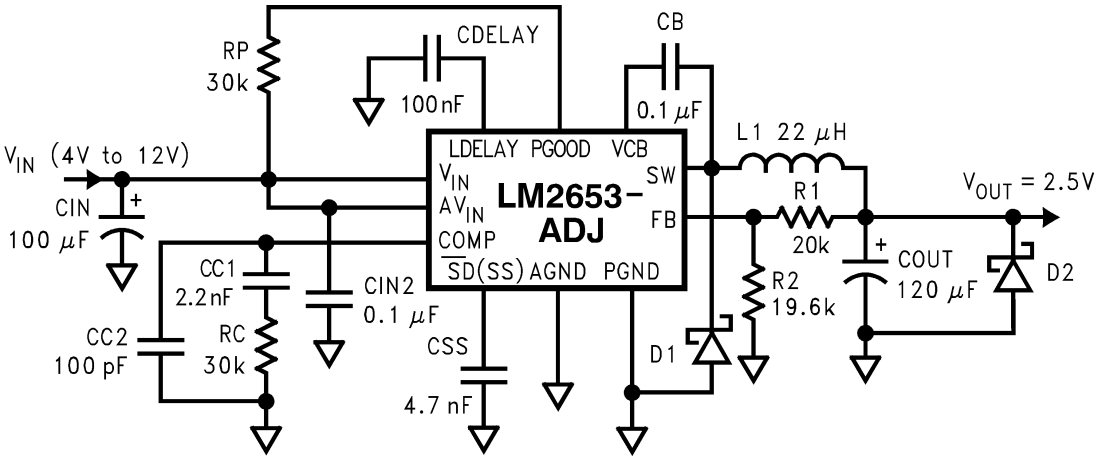

Figure 16. Schematic for the Typical Board Layout

Typical PC Board Layout: (2X Size)

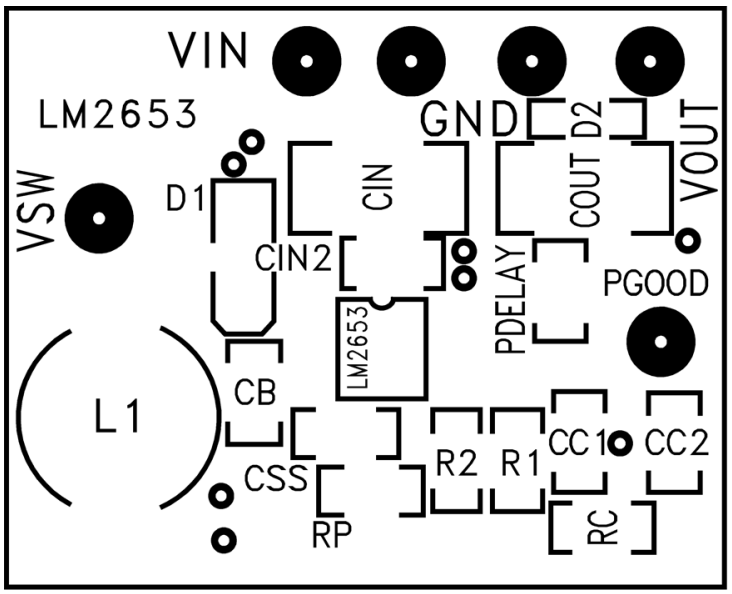

Figure 17. Component Placement Guide

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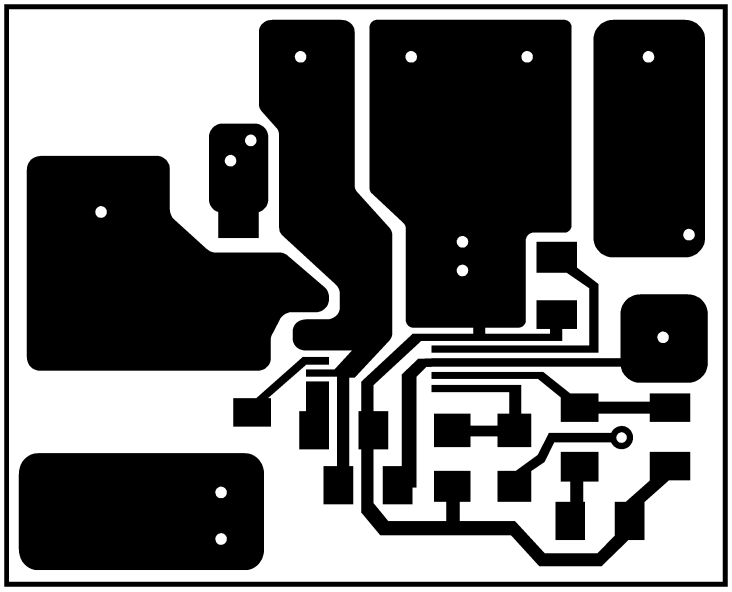

Figure 18. Component Side PC Board Layout

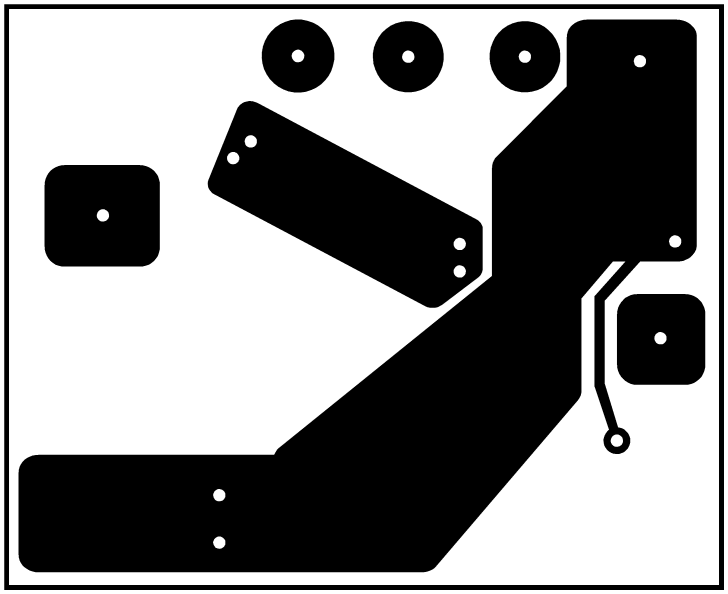

Figure 19. Solder Side PC Board Layout

REVISION HISTORY

Changes from Revision D (April 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	13

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2653MTC-ADJ	NRND	TSSOP	PW	16	92	TBD	Call TI	Call TI	-40 to 125	2653MT C-ADJ	
LM2653MTC-ADJ/NOPB	ACTIVE	TSSOP	PW	16	92	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	2653MT C-ADJ	Samples
LM2653MTCX-ADJ/NOPB	ACTIVE	TSSOP	PW	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	2653MT C-ADJ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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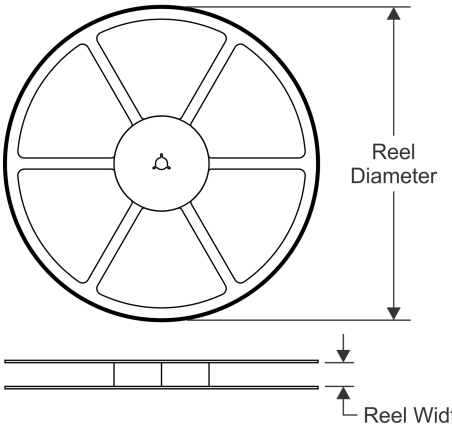
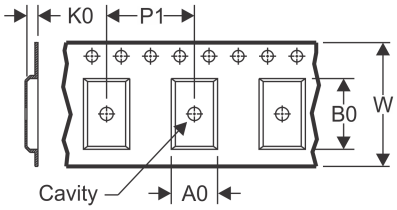
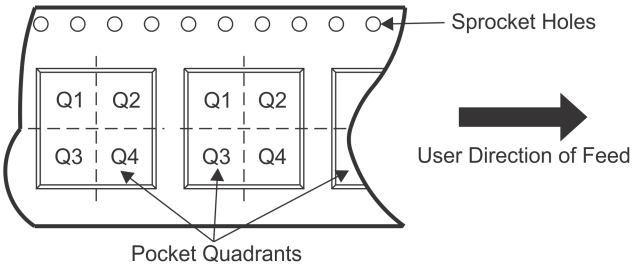


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

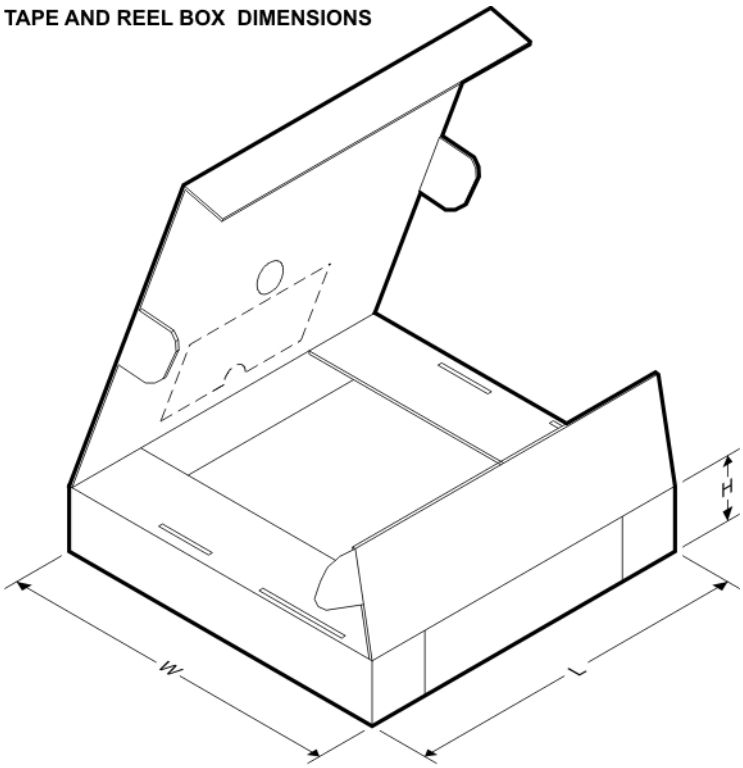
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2653MTCX-ADJ/NOPB	TSSOP	PW	16	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1

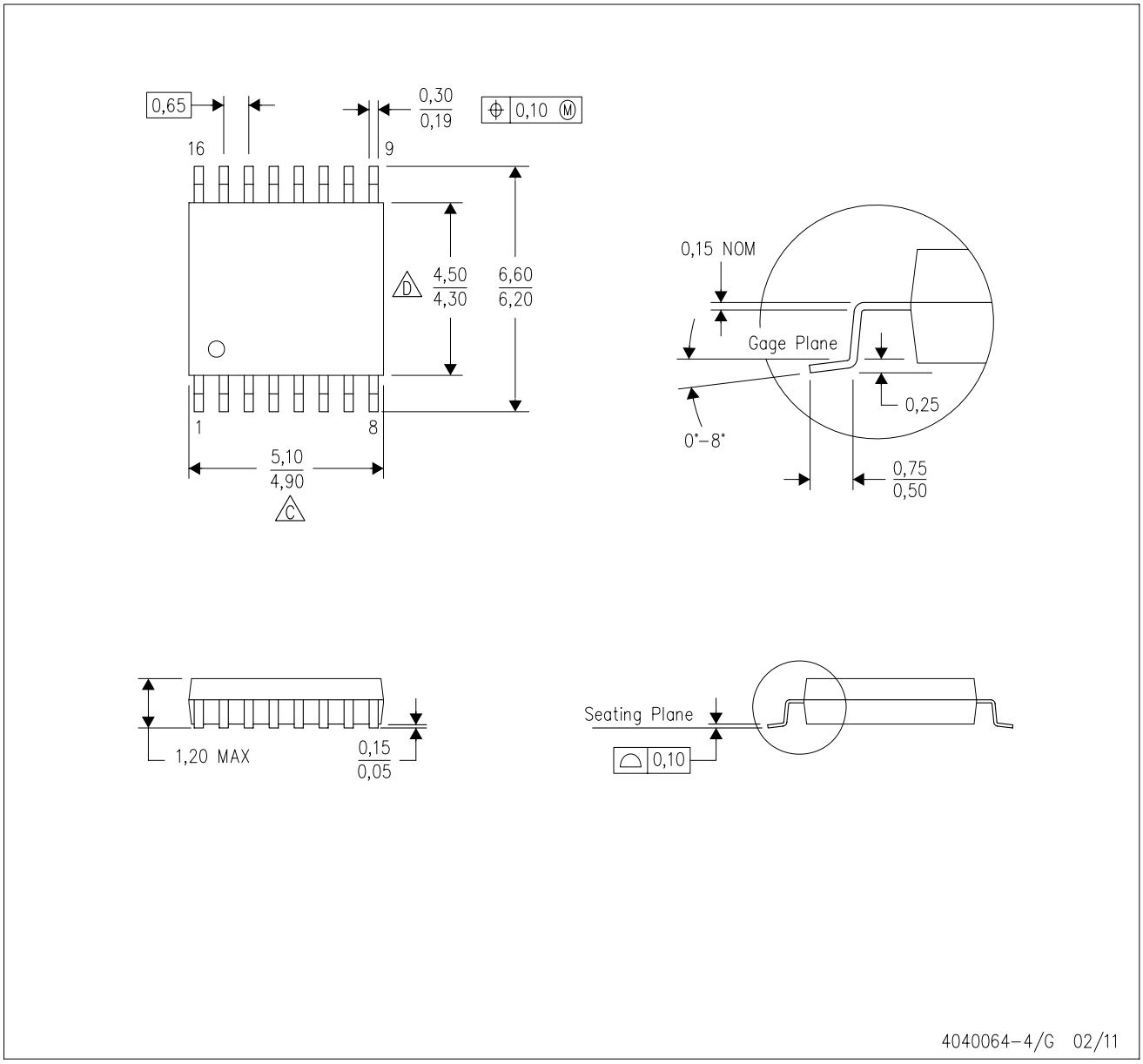
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2653MTCX-ADJ/NOPB	TSSOP	PW	16	2500	367.0	367.0	35.0

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

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